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AMDs Journey to Exascale

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With the Frontier and El Capitan systems on the horizon, ExaFLOP-sized systems have now become a reality. Manufacturers, HPC users, and with especial interest from weather community, are all now investigating how to most easily leverage hardware, software, and toolchains in order to scale problems and codes across this new generation of systems.

In this presentation the AMD HPC Centre of Excellence will discuss AMDs approach in this journey. With a brief synopsis of where we see the direction of travel for HPC to the middle of this decade we will discuss some methods of characterization of WRFv3, and how this lends itself to the CPU architecture (last level cache, memory) and AMD EPYC™ processors. We will then review AMDs approach to migrate codes from the CPU to the GPU through hardware like AMD Instinct™, open-source software development environment, and standardized programming paradigms (the OpenMP API "target" directives and the HIP programming model). We will also briefly present how to port existing codes to these programming paradigms.

Primary author: Mr GONTIER, Mathieu (AMD)

Presenter: Mr GONTIER, Mathieu (AMD)

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