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FPGA Acceleration of the LFRic Weather and Climate Model in the EuroExa Project Using Vivado HLS

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Mike Ashworth, Graham Riley, Andrew Attwood, and John Mawer
School of Computer Science, University of Manchester, Manchester M13 9PL, UK

The EuroExa project proposes a High-Performance Computing (HPC) architecture which is both scalable to Exascale performance levels and delivers world-leading power efficiency. This is achieved through the use of low-power ARM processors accelerated by closely-coupled FPGA programmable components. In order to demonstrate the efficacy of the design, the EuroExa project includes application porting work across a rich set of applications. One such application is the new weather and climate model, LFRic (named in honour of Lewis Fry Richardson), which is being developed by the UK Met Office and its partners for operational deployment in the middle of the next decade.

Much of the run-time of the LFRic model consists of compute intensive operations which are suitable for acceleration using FPGAs. Programming methods for such high-performance numerical workloads are still immature for FPGAs compared with traditional HPC architectures. We have selected the Xilinx Vivado toolset including High-Level Synthesis (HLS). HLS generates a block of code for the FPGA (an IP block) from a pure C, C++ or OpenCL function annotated with HLS pragmas, which supply optimization hints and instructions about the data interface. This block can be combined with other standard IP blocks in Vivado Design Studio and a bitstream generated for programming the FPGA. The FPGA is then driven by standard C code on the ARM processor which manages the flow of data between the ARM and the FPGA and handles signals to control the HLS blocks. We shall describe this process in detail, discuss the benefits of a range of optimizations and report performance achieved from a matrix-vector multiply kernel.

Affiliation

University of Manchester

Primary authors: Dr ASHWORTH, Mike (University of Manchester); Dr RILEY, Graham (University of Manchester); Dr ATTWOOD, Andrew (University of Manchester); Dr MAWER, John (University of Manchester)

Presenter: Dr ASHWORTH, Mike (University of Manchester)

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